a second conductive path disposed peripherally around said semiconductor chip, having a bonding pad shape;

a third conductive path having a shape of an external connecting pad and coupled to said second conductive path, **said third conductive path being disposed underneath said semiconductor chip and coupled to said semiconductor chip through an insulating material**;

connecting means for electrically connecting said semiconductor chip to said second conductive path;

insulating resin covering said semiconductor chip, filling in the trench, and integrally supporting the semiconductor chip and the conducive paths with a bottom surface of the paths exposed. (Emphasis added.)

The above bolded features, which were stressed in the previous response, were not addressed in the Final office action. To establish *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. *In re Royka*, 490 F.2d 981, 180 USPQ 580 (CCPA 1974). "All words in a claim must be considered in judging the patentability of that claim against the prior art." *In re Wilson*, 424 F.2d 1382, 1385, 165 USPQ 494, 496 (CCPA 1970). If an independent claim is nonobvious under 35 U.S.C. §103, then any claim depending therefrom is nonobvious. *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988). Here, the bolded features were not addressed or considered in the Final Office Action, and Applicants stress that they are not taught or suggested by the cited prior art references.

To reiterate, Fukutomi et al. in view of Fjelstad and Kweon et al. does not show a structure as claimed in claim 1 where the first conductive path, which is disposed underneath the semiconductor chip, is coupled to the semiconductor chip through a thermally conductive material, and the third conductive path, also disposed underneath the semiconductor chip, is coupled to the semiconductor chip through an insulating material.

Fukutomi et al. shows a die-bonding material 66 bonding the chip 65 to the wiring patterns 63 (see Fig. 22c). Fjelstad shows gold being selectively plated to the first surface 401 and bonded to the entire undersurface of the chip 420 (see Fig. 7D and column 8, lines 13 to 17). Kweon et al. shows an Ag-epoxy adhesive 120 dispose below the entire surface of the chip 110 (see Fig. 10). A combination of the cited prior art does not disclose, teach, or suggest a configuration as claimed in claim 1. That is, none of the cited references show two different conductive paths underneath the semiconductor chip with **one path coupled to the chip through a thermally conductive material and another path coupled to the chip through an**

**insulating material**. Thus, a person of ordinary skill in the art would not have found obvious the present invention of claim 1 by the combination of the cited prior art.

Claims 2, 3, 5 to 13 depend on claim 1 directly or indirectly. Therefore, these clams are also unobvious at least for the same reason as claim 1.

Claim 14 recites:

> 14. (Amended) A semiconductor device comprising:
> a plurality of conductive paths electrically separated from one another by a trench;
> **a semiconductor chip connected with at least one of said conductive paths through a thermal conductive material**; and
> insulating resin which covers said semiconductor chip, is embedded in the trench among said plurality of conductive paths and integrally supports the conducive paths, rear surface of which are at least partially exposed from the insulating resin,
> **wherein at least another one of said conductive paths is disposed at a periphery of said semiconductor chip and extends underneath the chip and coupled to the chip through an insulating material to form an external terminal.** (Emphasis added.)

Because claim 14 has similar limitations as claim1, claim14 would not have been obvious to a person of ordinary skill in the art at least for the same reason as claim 1. That is, the bolded features above are not disclosed, taught, or suggested by the cited prior art references.

Claims 15 and 16, which depend on claim 14, are also unobvious at least for the same reason as claim 14.

Furthermore, claim 12 is also not taught or suggested by the cited references. Claim 12 recites:

> 12. (Amended) A semiconductor device according to claim 1, wherein said first conductive path is coupled with a conductive pattern formed on a mounting board through a thermally conductive material.

This together with claim 1 states that the device has the following layered configuration: the semiconductor chip--thermally conductive material--the first conductive path--thermally conductive material-the conductive pattern. This configuration is not taught or suggested by any of cited prior art references.

New Claims

New claim 17 has similar features as claim 1. Thus, at least for the same reasons as claim 1, claim 17 are not obvious. The dependent claims are not obvious at least for the same reason as claim 17.

New claim 25 features "a conductive path comprising a first path extending under the semiconductor chip to form an external electrode and a second path extending from the first path and having a first face connected to the semiconductor chip and a second face provided as another external electrode." This feature is not disclosed, taught, or suggested by the cited prior art references.

Attached is a marked-up version of the changes being made by the current amendment.

Applicant asks that all claims be allowed. Please find enclosed a check for the claim fee. Please apply any other charges or credits to Deposit Account No. 06-1050.

Respectfully submitted,

Date: 1/29/03

Chris T. Mizumoto
Reg. No. 42,899

Fish & Richardson P.C.
45 Rockefeller Plaza, Suite 2800
New York, New York 10111
Telephone: (212) 765-5070
Facsimile: (212) 258-2291

## Version with markings to show changes made

In the claims:

Claims 17 to 25 have been added as follows:

17. (New) A semiconductor device comprising:

a semiconductor chip; and

a plurality of conductive paths electrically separated by a trench, the conductive paths comprising a die pad shape disposed below and substantially at the center of the semiconductor chip, an external connecting shape disposed below the semiconductor chip, and a bonding pad shape disposed beyond the semiconductor chip and being connected to the conductive path of the external connecting shape;

wherein the semiconductor chip is disposed over and coupled to the conductive path of the die pad shape through a thermally conductive material, and the conductive path of the external connection shape is coupled to said semiconductor chip through an insulating material.

18. (New) A semiconductor device according to claim 17, further comprising:

connecting means for electrically connecting said semiconductor chip to the conductive path of the bonding pad shape;

19. (New) A semiconductor device according to claim 17, further comprising:

an insulating resin covering said semiconductor chip, filling in the trench, and integrally supporting the semiconductor chip and the conducive paths with a bottom surface of the paths exposed.

20. (New) A semiconductor device according to claim 17 wherein the conductive path of the die pad shape has a smaller size than that that of the rear surface of said semiconductor chip, the conductive path of the external connecting shape is larger than the conductive path of the bonding pad shape.

21. (New) A semiconductor device according to claim 20, wherein the insulating material is provided between said wiring extended to the rear surface of said semiconductor chip and said semiconductor chip or between the conductive path of the external connecting shape and said semiconductor chip.

22. (New) A semiconductor device according to claim 17, wherein the side of each of said conductive paths is curved to mate with said insulating resin.

23. (Amended) A semiconductor device according to claim 17, further comprising:

a conductive film selectively covering said conductive paths and having made of material selected from the group consisting of nickel, silver and gold.

24. (New) A semiconductor device according to claim 17, wherein the conductive path of the die pad shape is coupled with a conductive pattern formed on a mounting board through a thermally conductive material.

25. (New) A Semiconductor device comprising:

a semiconductor chip;

a conductive path comprising a first path extending under the semiconductor chip to form an external electrode and a second path extending from the first path and having a first face connected to the semiconductor chip and a second face provided as another external electrode.